

REMARKS

Applicant's Response to Rejections Under 35 U.S.C. §103

Currently claims 1, 2, 13, 15, and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Nishimura et al.* (USP 5,736,438) in view of *Yamazaki et al.* (USP 5,824,574), and further in view of *Kawaguchi* (USP 6,245,622) and claims 3-8 further in view of *Talwar et al.* (USP 5,908,307), and further in view of *Noda et al.* (USP 6,432,802).

In addition, claims 9-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Nishimura et al.* in view of *Yamazaki et al.*, further in view of *Kawaguchi*, and further in view of *Yoshimi et al.* (USP 5,698,869), and claims 18, 20, 21-23, 25 and 26 stand rejected over these references further in view of *Noda et al.* Claims 27-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Nishimura et al.* in view of *Kawaguchi*, further in view of *Chong et al.* (USP 6,335,253).

In response thereto, applicant has amended independent claims 1, 3, 9, 13, 18 and 23 to more distinctly claim the subject matter which is regarded as the invention. Specifically, applicants have amended the claims to recite the limitation that the impurities are introduced into the amorphous regions of the single crystal semiconductor region. Applicant respectfully submits that none of the references cited teach or suggest the embodiments as claimed in amended claims 1, 3, 9, 13, 18 and 23.

The invention of amended independent claims 1, 3, 9, 13, 18 and 23 includes the steps of: introducing atoms, (e.g., germanium) to form amorphous regions seeping into a single crystal semiconductor region, and introducing impurities into the amorphous regions of the single crystal semiconductor region.

The laser annealing technique is used, which provides a sharp impurity profile. However, it is the principal object of the present invention that the laser annealing is performed after executing the above steps to obtain the sharp impurity profile without presenting an increase in parasitic resistance, which is clearly described in the present specification. (See specification, pages 14-20).

None of the cited references in this Office Action discloses or suggests the step of forming amorphous regions seeping into a single crystal semiconductor region under the gate. Further, none of the references indicates any introduction conditions as defined in claims 9 and 23 of the present invention.

Applicant respectfully submits, that in light of the amendment, that the prior art cited even when combined would not result in applicant's claimed invention. Wherefore, applicant respectfully requests removal of the rejections.

In addition to the arguments above, claims 27-30 contain the allowable limitation of claim 14, *i.e.*, the source side having a capacitance of 0.25 (fF/ μ m/side) or more. This limitation does not appear in the prior art. This result of 0.25 (fF/ μ m/side) capacitance is a surprising result of the particular embodiment (*see* specification, page 18). As such, Applicant respectfully requests removal of this rejection.

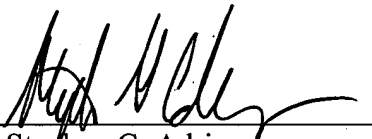
For at least the foregoing reasons, it is believed that this application is now in condition for allowance. If, for any reason, it is believed that this application is not in condition for allowance, Examiner is encouraged to contact the Applicants' undersigned attorney at the telephone number below to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully submitted,

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Attachments: Petition for Extension of Time w/Fee
Change of Correspondence Address
MJC/SGA/rer/ww